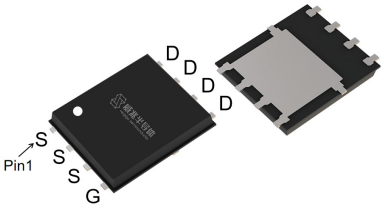
Features

- Enhancement mode
- Very Low on-resistance $R_{DS(on)}$
- VitoMOS® Ⅱ Technology
- 100% Avalanche test

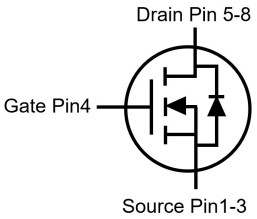
V_{DS}	40	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	3.4	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5V	5.1	mΩ
I_D	80	A

PDFN5x6



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VSP007N04MS-G	PDFN5x6	007N04M	3000PCS/Reel



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		40	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C=25°C	30	A
I_D	Continuous drain current @VGS=10V	T_C=25°C	80	A
		T_C=100°C	50	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	320	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	27	A
		T_A=70°C	22	A
EAS	Avalanche energy, single pulsed ②		45	mJ
P_D	Maximum power dissipation	T_C=25°C	36	W
		T_C=100°C	14	W
P_{DSM}	Maximum power dissipation ③	T_A=25°C	4.2	W
		T_A=70°C	2.7	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.5	4.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	30	36	°C/W

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Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=40V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.2	1.65	2.3	V
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=10V, I_D=30A	--	3.4	4.3	mΩ
		T_j=100℃	--	4.3	--	mΩ
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=4.5V, I_D=20A		5.1	6.4	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=20V,V_{GS}=0V, f=1MHz	975	1300	1730	pF
Coss	Output Capacitance		350	465	620	pF
Crss	Reverse Transfer Capacitance		35	50	70	pF
Rg	Gate Resistance	f=1MHz	0.5	1.4	5	Ω
Qg(10V)	Total Gate Charge	V_{DS}=20V,I_D=30A, V_{GS}=10V	--	27	36	nC
Qg(4.5V)	Total Gate Charge		--	14	19	nC
Qgs	Gate-Source Charge		--	4.1	5.5	nC
Qgd	Gate-Drain Charge		--	6.5	10	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=20V, I_D=30A, R_G=3Ω, V_{GS}=10V	--	6.6	--	ns
Tr	Turn-on Rise Time		--	64	--	ns
Td(off)	Turn-Off Delay Time		--	23.4	--	ns
Tf	Turn-Off Fall Time		--	17	--	ns
Source- Drain Diode Characteristics@ T_j= 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=30A,V_{GS}=0V	--	0.8	1.2	V
Trr	Reverse Recovery Time	T_j=25℃,I_{sd}=30A, V_{GS}=0V di/dt=100A/μs	--	28	56	ns
Qrr	Reverse Recovery Charge		--	13	26	nC

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.1mH, R_G = 25Ω, I_{AS} = 30A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle≤ 2%.

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Typical Characteristics

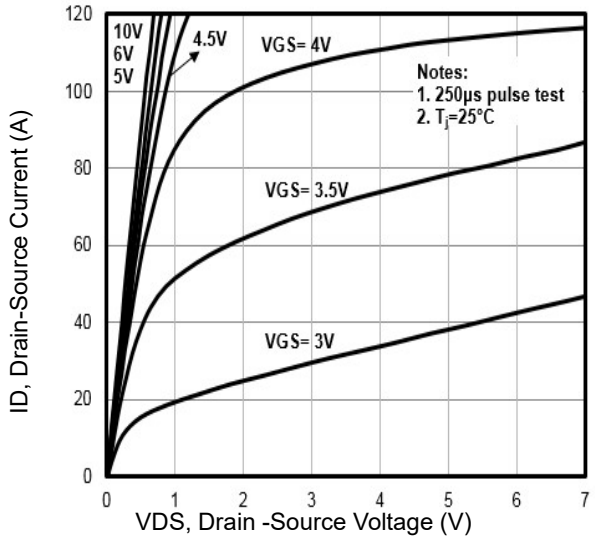


Fig1. Typical Output Characteristics

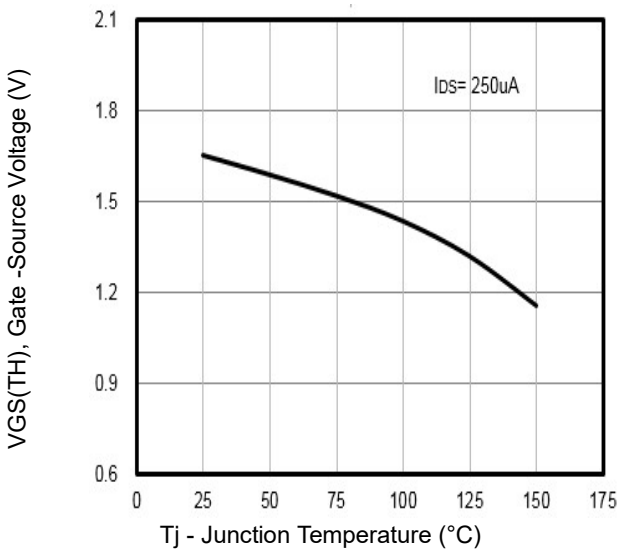


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

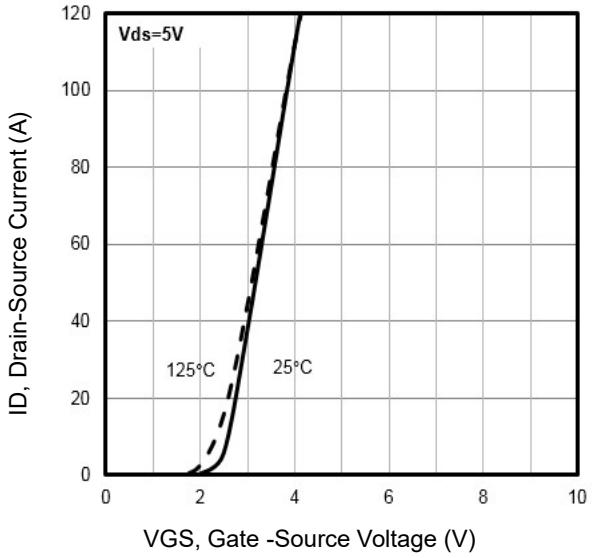


Fig3. Typical Transfer Characteristics

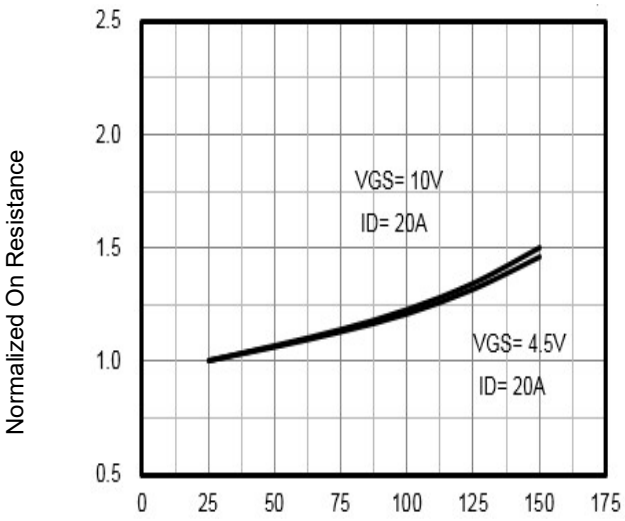


Fig4. Normalized On-Resistance Vs. Tj

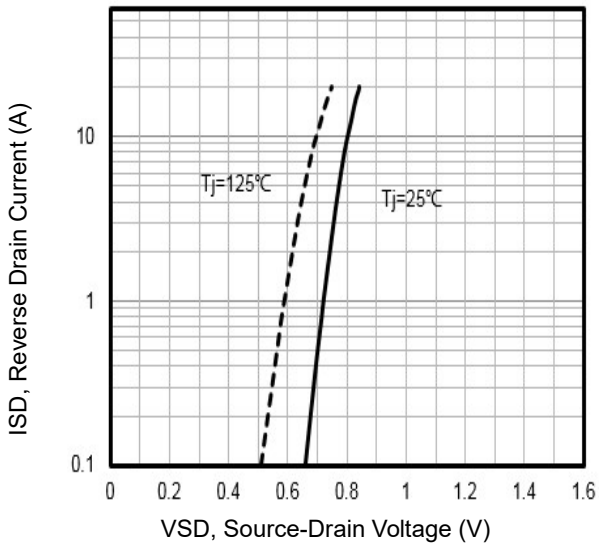


Fig5. Typical Source-Drain Diode Forward Voltage

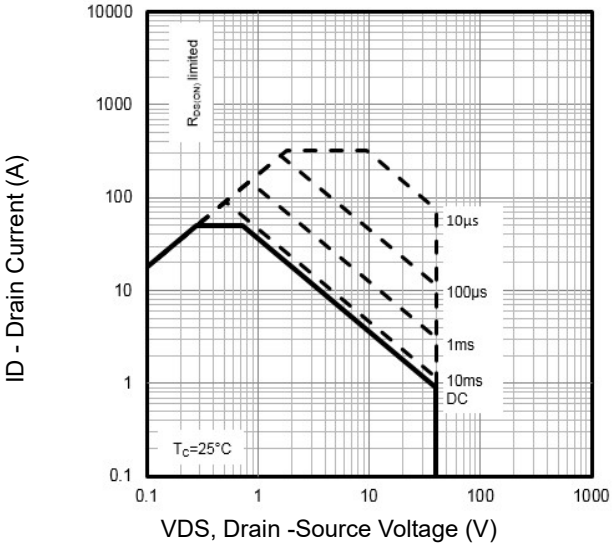


Fig6. Maximum Safe Operating Area

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Typical Characteristics

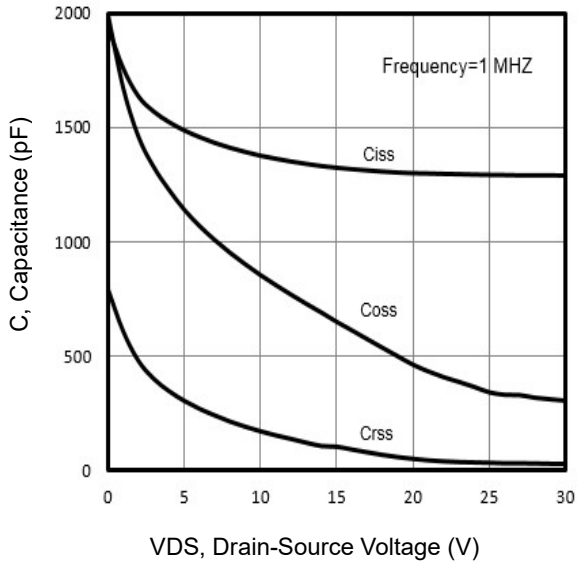


Fig7. Typical Capacitance Vs. Drain-Source Voltage

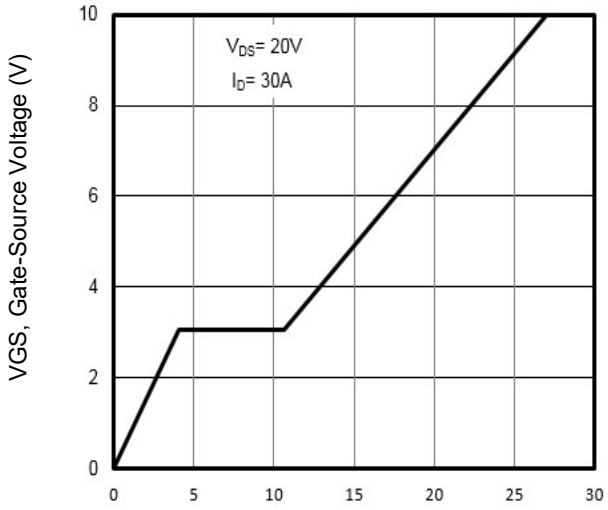


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

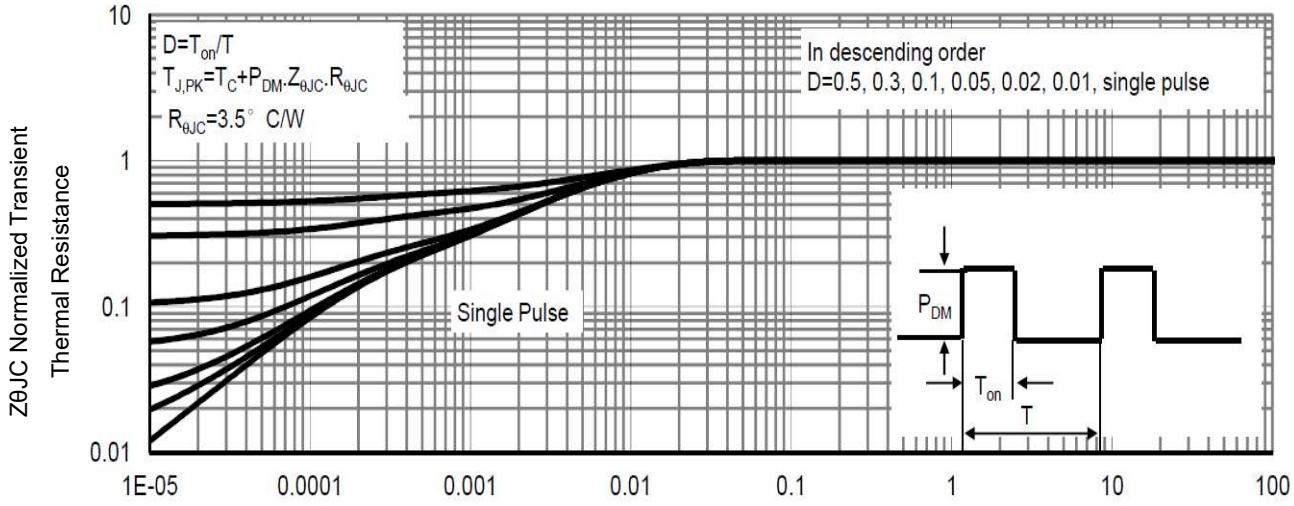


Fig9. Normalized Maximum Transient Thermal Impedance

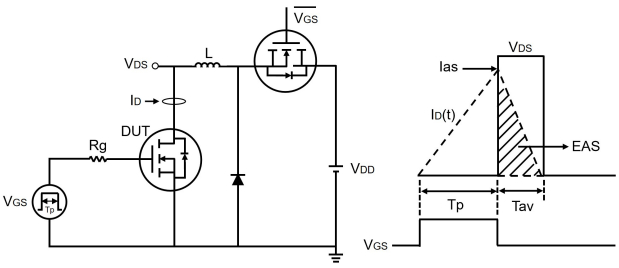


Fig10. Unclamped Inductive Test Circuit and waveforms

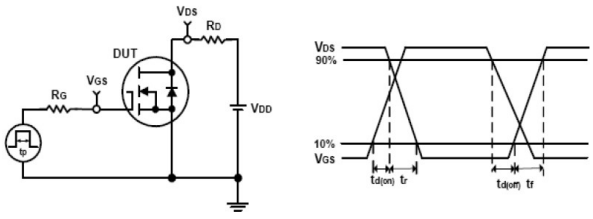
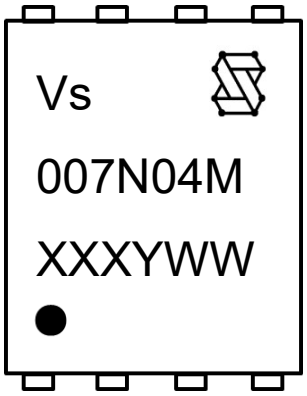


Fig11. Switching Time Test Circuit and waveforms

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Marking Information

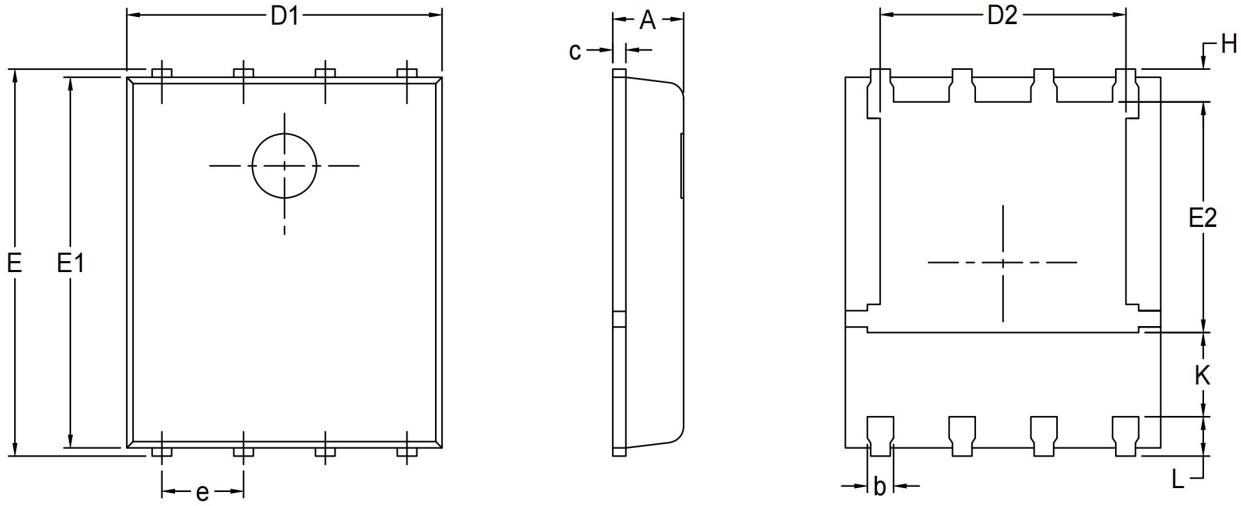


1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（007N04M）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code, code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

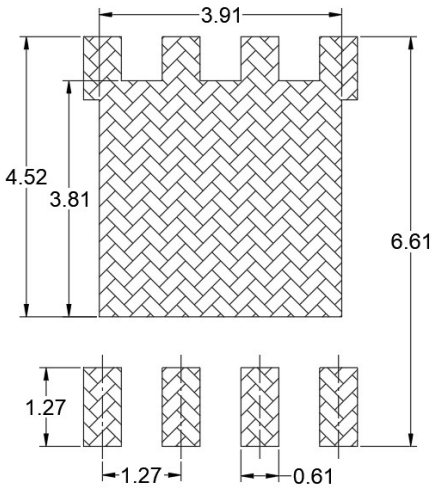
Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

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PDFN5x6 Package Outline Data



Land Pattern
(Only for Reference)



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71

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